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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,954	06/09/2004	Kwun-Yao Ho	11530-US-PA	3953
31561	7590	09/29/2005	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.D

Office Action Summary	Application No.	Applicant(s)	
	10/709,954	HO ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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Serial Number: 10/709954 Attorney's Docket #: 11530-US-PA

Filing Date: 6/9/2004; claimed foreign priority to 8/14/2003

Applicant: Ho et al.

Examiner: Alexander Williams

Applicant's election of species III, figures 4A-4H, claims 1-11 filed 9/9/05 from the previous election of Group I (claims 1 to 11), filed 7/25/05, has been acknowledged.

Claims 12-30 have been cancelled.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to because the drawing fail to show that the conductive vias and the barrier layers are made of gold. This would show being the same material?

Correction is required.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

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art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 to 11 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the barrier layer and the conductive vias, does not reasonably provide enablement for both being made of a material such as gold. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to understand the invention commensurate in scope with these claims. How is the **barrier layer** 304a and the **conductive vias** 304b both fabricated using a conductive material such as **gold**? See paragraph [0035]. Is this correct? Please explain.

Any of claims 1 to 11 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 7 and 9 to 11, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Shimoto et al. (U.S. Patent # 6861,757 B2).

1. Shimoto et al. (figures 1 to 18d) specifically figure 3 show an electrical package comprising: a multi-layer interconnection structure **6** having a top surface, a bottom surface and an inner circuit therein, wherein the inner circuit has a plurality of bonding pads **5,8** on the bottom surface of the multi-layer interconnection structure; at least an electronic device (**not shown in figure 3, but shown in figure 9 as 18**) positioned on the top surface of the multi-layer interconnection structure and electrically connected to the inner circuit of the multi-layer interconnection structure; and a support substrate **16** made from a conductive material, wherein the support substrate is positioned on the bottom surface of the multi-layer interconnection structure, and the support substrate has a plurality of first openings that exposes one of the corresponding bonding pads.

ABSTRACT :

An interconnecting substrate for carrying a semiconductor device, comprising: an insulating layer; an interconnection set on an obverse surface of the insulating layer; an electrode which is set on a reverse surface side of the insulating layer and formed in such a way that, at least, a lateral face of an obverse end of the electrode is all round brought into contact with the insulating layer, while, at least, a reverse surface of the electrode is not in contact with said insulating layer; a via conductor which is disposed on an obverse surface of the electrode and formed in the insulating layer so as to connect this electrode with the interconnection; and a supporting structure on the surface of the insulating layer.

2. The electrical package of claim 1, Shimoto et al. show wherein the package further comprises an isolation layer 17 made from an insulation material such that the isolation layer is disposed between the mold-layer interconnection structure and the support substrate and that the isolation layer has a plurality of second openings that exposes one of the corresponding bonding pads.

3. The electrical package of claim 1, Shimoto et al. show wherein each bonding pad has a barrier layer thereon such that the barrier layer is exposed by the first opening.

(77) Further, the present invention relates to a method of producing an interconnecting substrate for carrying a semiconductor device as set forth above, wherein, in formation of said electrode pattern, there is formed a layered structure of said electrode pattern in which a Cu layer is disposed in an obverse end section, a barrier conductive layer to prevent diffusion of solder is disposed on a reverse end side thereof, and a barrier conductive layer to etching removal of said substrate is disposed on a further reverse end side thereof.

4. The electrical package of claim 1, Shimoto et al. show wherein the electronic device comprises a die, a passive component or an electrical package.

5. The electrical package of claim 1, Shimoto et al. show wherein material constituting the support substrate comprises a metallic material or an alloy (see column 9, line 53 to column 10, line 43).

(15) The material of the supporting structure is not specifically limited as far as it can provide the interconnecting substrate a sufficient strength as

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described above and have a heat resistance strong enough to stand heat treatments performed at the time of loading the semiconductor chip onto the interconnecting substrate and mounting the interconnecting substrate or the package of the semiconductor device, but the conductive material is preferably used from the viewpoint of producing the electrodes, via conductors and interconnections. For the conductive material of this sort, metal made of stainless steel, copper, copper alloy, aluminium, nickel or such is preferably employed because of its availability at low cost, easiness to work into shape, and, what is more, sufficient mechanical strength.

6. The electrical package of claim 1, Shimoto et al. show wherein the package further comprises a plurality of contacts connected to various bonding pads through corresponding first openings.

7. The electrical package of claim 6, Shimoto et al. show wherein the contacts are configured as solder balls, pins or electrode blocks.

9. The electrical package of claim 1, Shimoto et al. show wherein the package further comprises at least an insulation layer **17** disposed over a sidewall of at least one of the first openings.

10. The electrical package of claim 1, Shimoto et al. show the package further comprises a solder mask layer **17** disposed over a sidewall of at least one of the first openings.

11. The electrical package of claim 1, Shimoto et al. show wherein the electronic device **18** is electrically connected to the inner circuit within the multi-layer interconnection structure through **flip-chip bonding**, wire-bonding or a thermal pressure bonding.

Claims 1 to 4 and 6 to 11, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Bohr (U.S. Patent # 6,617,681 B1).

1. Bohr (figures 1 to 21) specifically figures 3 and 1 show an electrical package **115** comprising: a multi-layer interconnection structure **120** having a top surface, a bottom surface and an inner circuit therein, wherein the inner circuit has a plurality of bonding pads on the bottom surface of the multi-layer interconnection structure; at least an

electronic device (inherent, shown in figure 1) positioned on the top surface of the multi-layer interconnection structure and electrically connected to the inner circuit of the multi-layer interconnection structure; and a support substrate **116** made from a conductive material, wherein the support substrate is positioned on the bottom surface of the multi-layer interconnection structure, and the support substrate has a plurality of first openings that exposes one of the corresponding bonding pads.

2. The electrical package of claim 1, Bohr show wherein the package further comprises an isolation layer **120** made from an insulation material such that the isolation layer is disposed between the multi-layer interconnection structure and the support substrate and that the isolation layer has a plurality of second openings that exposes one of the corresponding bonding pads.

3. The electrical package of claim 1, Bohr show wherein each bonding pad has a barrier layer thereon such that the barrier layer is exposed by the first opening.

4. The electrical package of claim 1, Bohr show wherein the electronic device comprises a die, a passive component or an electrical package.

6. The electrical package of claim 1, Bohr show wherein the package further comprises a plurality of contacts connected to various bonding pads through corresponding first openings.

7. The electrical package of claim 6, Bohr show wherein the contacts are configured as solder balls, pins or electrode blocks.

8. The electrical package of claim 6, Bohr show wherein at least one of the contacts completely fills the first opening so that the contact is electrically connected to the support substrate.

9. The electrical package of claim 1, Bohr show wherein the package further comprises at least an insulation layer **120** disposed over a sidewall of at least one of the first openings.

10. The electrical package of claim 1, Bohr show the package further comprises a solder mask layer **120** disposed over a sidewall of at least one of the first openings.

11. The electrical package of claim 1, Bohr show wherein the electronic device (inherent, but shown in figure 1) is electrically connected to the inner circuit within the

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multi-layer interconnection structure through **flip-chip bonding**, wire-bonding or a thermal pressure bonding.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/778,737,734,738,700,701,712,713,717,720,675,696,6 98,692,693,691	9/27/05
Other Documentation: foreign patents and literature in 257/778,737,734,738,700,701,712,713,717,720,675,696,6 98,692,693,691	9/27/05
Electronic data base(s): U.S. Patents EAST	9/27/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/27/05